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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,670	04/14/2004	Won Sun Shin	GK0012RI	8344

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,670	SHIN ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin et al. (U.S. 6,515,356 B1).

Shin discloses a semiconductor package with

(1) providing a circuit board strip (10) including a plurality of unit circuit boards (10) each unit circuit board having a plurality of first ball lands (15) formed at a first major surface thereof, a plurality of bond fingers (6) formed at an opposite second major

surface thereof, vias through the circuit board (10) each electrically connected between a bond finger (6) and a first ball land (15), and a through hole between the first and second major surfaces;

receiving in each through hole a semiconductor chip (2) having a first major surface, and an opposite second major surface provided with a plurality of input/output pads (4) thereon, wherein the second major surface of the chip (2) faces in the same direction as the first major surface of the respective circuit board (10) (see Figure 6);

electrically connecting into input/output pads (4) of each semiconductor chip (2) with associated ones of the bond fingers (6) of the respective circuit board (10);

encapsulating (20) the semiconductor chips (2), and filling the through hole of each unit circuit board of the circuit board strip (10) using an encapsulating material (20);

fusing conductive balls (30) on the first ball lands (15) of each unit circuit board (10) (see Figure 6);

singulating the circuit board strip into semiconductor packages respectively corresponding to the unit circuit boards;

(2) wherein the circuit board strip comprises: a main strip including a resin substrate having a substantially rectangular strip shape, a first major surface and a second major surface;

a plurality of main slots extending to a desired length in a direction transverse to a longitudinal direction of the main strip while being uniformly spaced apart from one

another in the longitudinal direction of the main strip thereby dividing the main strip into a plurality of sub-strips aligned together in the longitudinal direction of the main strip;

a plurality of sub slots extending to a desired length and serving to divide each of the sub-strips into a plurality of strip portions arranged in a matrix array, each of the strip portions corresponding to one of the unit circuit boards having one of the through holes;

a plurality of first circuit patterns each formed on the first major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the first ball lands;

a plurality of second circuit patterns each formed on the second major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the bond fingers;

cover coats respectively coated over the first and second major surfaces of the rosin substrate while allowing the bond fingers and the ball lands to be exposed there-through (see Figure 6);

(3) wherein the circuit board strip comprises: a resin substrate having a substantially rectangular strip shape provided with a first major surface and a second major surface;

a plurality of slots extending to a desired length and serving to divide each of the resin substrate into a plurality of substrate portions arranged in a matrix array, each of the substrate portions corresponding to one of the unit circuit boards having one of the through holes;

a plurality of first circuit patterns each formed on the first major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the first ball lands;

a plurality of second circuit patterns each formed on the second major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the bond fingers;

cover coats respectively coated over the first and second major surfaces of the resin substrate while allowing the bond fingers and the ball lands to be exposed there-through (see Figure 6);

(4) further comprising attaching one or more closure members to the first surface of the substrate strip so that each through hole is covered thereby prior to receiving the semiconductor chip in the respective through hole (see Figure 6);

(5) further comprising: attaching a plurality of closure members to the first major surface of the circuit board strip in such a fashion that the closure members simultaneously cover associated ones of the through holes, prior to the step of receiving the semiconductor chips in the through holes (see Figure 6);

(6) further comprising the step of: attaching a plurality of closure members to the first major surface of the circuit board strip in such a fashion that the closure members simultaneously cover associated ones of the through boles, prior to the step of receiving the semiconductor chips in the through holes (see Figure 6);

(7) wherein attaching the closure member comprises: preparing closure member strips each having closure members for an associated one of the sub-strips;

individually attaching the closure member strip to the sub-strips, respectively, in such a fashion that each of the closure member strips is arranged to cover the main slot formed at one side of an associated one of the sub-strips (see Figure 6);

(8) wherein attaching the closure member comprises: preparing a single closure member strip having closure members for all sub-strips of the circuit board strip while having small singulation apertures at a region corresponding to each of the main slots;

attaching the closure member strip to the main strip in such a fashion that the closure member strip is arranged to allow each of the small singulation apertures to be aligned with an associated one of the main slots (see Figure 6);

(9) wherein the one or more closure members are removed after encapsulating the semiconductor chips (see Figure 6);

(10) wherein the closure members are removed after encapsulating the semiconductor chips (see Figure 6);

(11) wherein the closure members are removed after encapsulating the semiconductor chips (see Figure 6);

(12) wherein the closure members are removed after encapsulating the semiconductor chips by inserting a bar into one or more of the main slots in a direction from the second major surface of the circuit board strip to the first major surface of the second board strip,

thereby detaching an associated one of the closure members from the circuit board strip at one side of the associated closure member (see Figure 6);

(13) wherein the closure members are removed after encapsulating the semiconductor chips by inserting a bar into one or more of the main slots in a direction from the second major surface of the circuit board strip to the first major surface of the second board strip, thereby detaching an associated one of the closure members from the circuit board strip at one side of the associated closure member (see Figure 6);

(14) wherein each closure member is selected from the group consisting of an insulating tape, an ultraviolet tape, and a copper layer;

(15) wherein each of the closure members selected from the group consisting of an insulating tape, an ultraviolet tape, and a copper layer;

(16) wherein each of the closure members is selected from the group consisting of an insulating tape, an ultraviolet tape, and a copper layer;

(17) wherein a unitary body of encapsulant material covers the second major surface of all of the unit circuit boards of the circuit board strip (see Figure 6);

(18) wherein a unitary body of encapsulant material covers the second major surface of all of the unit circuit boards of the circuit board strip(see Figure 6) ;

(19) wherein a unitary body of encapsulant material covers the second major surface all of the unit circuit boards of the circuit board strip (see Figure 6);

(20) wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split;

(21) wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split;

(22) wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split;

(23) wherein encapsulating the circuit board strip comprises: interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity;

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface (see Figure 6);

(24) wherein the encapsulating the circuit board strip comprises: interposing the circuit board strip between a pair of mold dies one of which has cavities and gates in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity;

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface (see Figure 6);

(25) wherein the encapsulating the circuit board strip comprises: interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity;

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface fills the through hole, and contacts the closure member (see Figure 6);

(26) wherein the encapsulating the circuit board strip comprises: interposing the circuit board strip between a pair of mold dies one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity;

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface fills the through hole, and contacts the closure member (see Figure 6);

(27) wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof (see Figure 6);

(28) wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof (see Figure 6);

(29) wherein each unit circuit board of the circuit board strip further provided with a plurality of second ball lands at the second major surface thereof (see Figure 6);

(30) further comprising fusing a plurality of conductive balls on the second ball lands (see Figure 6);

(31) further comprising fusing a plurality of conductive balls on the second ball lands (see Figure 6);

(32) further comprising fusing a plurality of conductive balls on the second ball lands (see Figure 6);

(33) wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof (see Figure 6);

(34) wherein the one or more closure members are removed after encapsulating the semiconductor chips (see Figure 6);

(35) further comprising fusing a plurality of conductive balls on the second ball lands (see Figure 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
September 30, 2005